Key Factors on CSP Assembly Reliability

Reza Ghaffarian
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California
818-354-2059
Reza. Ghaffarian@JPL.NASA.Gov

Abstract

Although the weakest link of **CSP assembly reliability** has been often internal package failure, solder joint fatigue is still considered to be the key factor for reliability. Other key factors that affect solder joint reliability including package type, package build, board design, assembly variables, and accelerated environmental testing are also discussed. The reasons for unrealistic life projections for CSP assembly reliability by numerous modelers is also examined. It was concluded that availability of meaningful assembly reliability test results are needed to accelerate implementation of this technology. The JPL-led CSP consortium is addressing many of these issues.

Electronics Miniaturization Trends

Surface mount electronic packages are mounted directly onto the surface rather than inserting the leads into plated through-holes (PTHs). There are several surface mount package styles, both active and passive. Active devices are divided into those with terminations of leads on the periphery of the component, two or four sides, and those with terminations (either pads or solder bumps) over much of the bottom of the component. Peripheral Array Packages (PAP) have less potential for significant size reduction with increased I/O counts compared to Area Array Packages (AAPs).

Ball Grid Arrays (BGAs) from the latter category are now the mainstay alternative to PAPs. For example, the CSP version of the two sided PAP is the Lead-On-Chip (LOC) package and the version for AAPs are micro- (or mini-, fine pitch) BGA packages, generally with eutectic solder balls.

The CSP packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. Although CSP is defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die, many manufacturers refer to the package that is a miniaturized version of the previous generation.

Microelectronics Assembly Reliability

For surface mount, solder has both electrical and mechanical functions. Thus for SMT, damage to solder could readily affect functional integrity of the system. Therefore, defects that cause changes either in mechanical or electrical system characteristics and their reasons for failure are critical. The most common damage to solder joints are those induced by thermal cycling. The main cause of such damage is considered to be differences in thermal expansion of package and PWB materials. This is especially true for eutectic solder (63Sn/37Pb) which creeps at room temperature.

Creep for materials generally occurs at temperatures above half of the absolute melting temperature (T/T_m >0.5). This value is 0.65 at room temperature for eutectic solder. Creep and stress relaxation are main causes of cycling damage.

Thermal cycling induced damages are expected to increase even more with the trend toward energy conservation. Powering down whenever the system is not actively used results in more cycles. Previously, electronic hardware was generally left on for long periods of time which resulted in relatively few thermal cycles. The on-off demand raises more concerns regarding solder joints which are affected by thermal cycling. Thermal damage to solder joints are most often caused by the followings:

- Global CTE (Coefficient of Thermal Expansion) mismatch between the package and board induces stresses. The package and board can also have temperature gradients through the thickness and at surface areas
- Local CTE mismatch between solder attachmed to the component and the PWB

Reducing the CTE mismatch of components and PWBs reduces cycling damages, but the ideal condition depends on thermal conditions of the component, PWB, and solder. An ideally CTE matched condition could be a tailored PWB material with a slightly higher CTE value than the component. This is based on the assumption that the global CTE mismatch is dominant, and the component with the heat generating die is hotter than the PWB.

There are other approaches to reducing damage to solder joints. Underfill application is a common technique which has been widely used for direct attachment of chip on board or when package leads are not robust. Other less conventional approaches are aimed at absorbing CTE mismatch between the die and board within the package or externally through strain absorbing mechanisms, and therefore reducing stresses on the solder interconnects. These approaches could introduce their own unique damage since the weakest link now is transferred from solder to other areas of the attachment system.

Tests Methods for Reliability Evaluation

Thermal cycling and a series of other environmental tests have been commonly used to gain confidence in reliability of SM package and assemblies. There are also additional tailored tests for specific applications. For space applications, vibration and shock representation of launch is an example of a tailored experiment. For portable products, new tests are being carried out. Bend, drop, and perhaps "washing machine" tests are especially important. It is interesting to note that these tests are devised to meet the harsh environment generated by human mishandling. Customer perception of quality and reliability of products might become a reality, though these tests might not have any scientific basis.

CSP Assembly Thermal Cycling Data

Tables 1-3 show thermal cycles to failure under different conditions for various CSPs with low to high I/Os. Except for μBGA™, most other test results are from package manufacturers. Although manufacturer data are valuable, they are probably have been generated for chosen packages under extreme control and they might not represent user application environments.

Note from the Table 1 that for μBGA™, two user showed 1,000 and 500 failure cycles in the range of -55°C to 125°C. The higher value possibly were from a more controlled environment whereas the lower value represented a mix of different supplier licensees for this package. Among the grid array packages, the JACS-Pak™ is the only package which shows higher than 1,000 cycles to failure in the same temperature range. Ceramic CSPs show much closer reliability to this than their SM version. Reasons may include reduction in size and thickness. Strain induced on the ceramic joint directly related to size or Distance to Neutral Point (DNP). Note again that these data were generated by suppliers and there are no independent validation tests by others as yet.

Wafer level assemblies have often very low cycles to failure and most of them required underfilling to have comparable reliability to conventional SM packages. Leaded CSPs, with low I/O generally have comparable reliability to their SM counterparts as shown in Table 3. There is a large difference between the two independent sets of data for TSOP (Thin Small Outline Package). The two extremes are 200 and 2,200 failure cycles in the range of -55°C to 125°C.

A recent assembly characterization by a user revealed much valuable information (K. Newman, Chip Scale International '98). Most packages failed early and did not meet the user requirement for cycles to failure. Only two out of eight packages, from six manufacturers, passed the user failure free cycles requirement. Acceptable failure-free cycles was 3,500 cycles for thermal cycling in the range of 0°C to 100°C. The results were at least an order of magnitude lower that those for Plastic BGAs (PBGAs). Failures lower than 1,000 cycles, even in the range 0°C of 100°C, is a good indication of package immaturity at the time of evaluation (late 1997).

It is difficult to determine if use of underfill might have relieved these early failures since no information by package manufacturers was given. Detailed failure mechanism analyses might have revealed that use of underfill would reduce the number of failures. Underfilling was considered to be unacceptable because adding additional assembly steps.

VARIABLES AFFECTING CSP RELIABILITY

There are many other factors that affect CSP reliability. These include design, package build, solder paste, assembly, underfill, and type of test for reliability evaluation. In the following a few of these variables are discussed.

Design

- PWB pad design; For BGAs, discussions on use of solder mask defined vs. non-solder mask (SMD vs. NSMD) were hot subjects for a short period. There were two camps, one showing the improvement due to use of SMD– reasoning that masks over copper are needed for improved adhesion as well as the potential benefit of cycles to failure increased due to increase solder joint height. The other camp showed that crack initiation in solder, due to overlaying of the mask, could reduce the number of cycles to failure. NSMD is now commonly recommended.

  The pad size design relative to package has its own supporters. As a rule of thumb, the board pad size should be the same as the package. A slight unbalance in this relationship could result in failure at the board or package. Optimized conditions might differ for different packages depending on the ball attachment configuration.

Package Variables

- Die bond on interposer; There are various techniques that are used to transfer the die I/O to the interposer within the package. Each element of the package internal form has its own effect. For TAB CSP (Tape Automated Bonding), the TAB is the weakest link. For flip chip die in Jacs-Pak, the failure was observed on the C5 (board level) solder joint interconnection, when subjected to thermal cycling.

This might not be the general case for the flip chip die. CSPs and BGAs with flip chip dies are more susceptible to internal package failure than their wire bond versions.

- Interposer thickness; When the interposer was increased from 0.4 mm thickness to 0.6 mm, cycles to failure increased from 400 to about 800 cycles (-25/125°C). Data for Jacs-Pak™, indicates that semi-rigid interposer would have 1.88 times the number of thermal cycles. Is the rigidity equivalent to thickness change or possibly because of materials change? The answer is not known. Interposer CTE also has significant affect on the board reliability.
- Interposer materials- CSPs with different interposer materials showed significantly different cycles to failure– about a three times increase (Sony, IMAPS '97). In an experiment verified by theoretical modeling, it was found that a factor of about three times will be achieved when a low CTE interposer was used (3000 vs. 800 cycles, -40/125°C, N_f 50%).
- Die size; In one study it was shown (Amkor, ECTC 98) that when die size increased from 6.4 mm to 9.5 mm, the first cycles to failure decreased from 1500 to 900 cycles in the range of -40°C to 125°C.

Solder Ball

Solder composition; Eutectic solder (63/37) is the most commonly used solder due to it having many desirable attributes, including low temperature melting. To improve fatigue characteristics, small amounts of silver (2%) have been added to this composition. Additive materials have the potential of formation of brittle intermetallic phases as well as softening by precipitation formation. These metallurgical transitions are further accelerated by increases in temperature. Effect of five element alloy was shown to improve thermal cycling reliability by 1.2 to 1.5 times (TI, SMI '97).

Ball shape attachment; For BGAs, it has been demonstrated that the DBGAs (Dimple BGA) improve reliability. This might be the case for CSPs too, but its significance is yet to be demonstrated.

Assembly Variables of Reliability

Solder joint height; The effect of solder joint height on reliability has been widely discussed for BGAs. One reason for the use of an SMD pad for PBGAs, with collapsible solder, was to increase solder ball height and hence increase reliability. Height was also increased by use of columns in the ceramic column grid arrays to achieve significant reliability improvements compared to the ball grid array version. Improvement was shown for CSPs when ball heights are increased (Son, IMAPS 97). When solder height is doubled, cycles to failure for the board tripled– a Coffin-Manson exponential value of β=1.6.

Underfill; One key advantage of CSPs over flip chips is that ideally there is no requirement for CSPs to be underfilled. The assemblers for consumer products prefer packages with no underfill one process step is eliminated and reworkability is permitted. However, for high reliability applications where vibration and shock are key in ruggedness, use of underfill might be the only solution now known to meet the harsh requirements.

For flip chips with very short cycles to failure, it has been shown that underfill will improve cycles to failure reliability an order of magnitude (5-10 at least). This is very similar to the results shown in Table 2 for the wafer level miniBGA packages with and without underfill.

Double Reflow; There are many concerns when double sided boards are assembled. Reliability reduction is one. For heavy BGAs, one concern was potential part fall from the assembled side during the second reflow. Similar concerns might be true for CSPs with the small solder volume; not enough tension force to hold even the small size of CSPs. In addition, it has been shown that for two sided packages, reliability of board assembly was half of the single sided (Sony, IMAPS '97). Recently, similar test results were presented for another CSP package (Sharp, ECTC 98). Double sided assemblies with packages on directly opposite sides of the board showed lower cycles to failure. This was improved with partial relative package offsets on the two sides.

Failure Mechanisms and CSP Reliability

Solder joint interconnects were considered to be the main cause of assembly failure. Failure at the board level could also be caused by the internal failure of the package. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP— a fatigue failure shift from the solder joint to the internal package (see Table 1). This new type of failure is in contrast to the traditional theoretical wisdom where the solder joint failure is generally considered to be the weak link in solder joint assemblies. This and other failure mechanisms, which are being established for CSPs, must be understood by a modeler before he/she is to predict a meaningful reliability projection.

Table 4 includes four projections from different modelers and experiment test results. It is interesting to compare the theoretical values with those experiment test results for numerous CSPs. It becomes obvious that these calculation are at least 5 to 20 times higher than the test results. As noted earlier, the highest value test results are in the range of 1,000 to 1,500 cycles. Projections of more

than 20,000 cycles to failure in the range of -55 to 125°C is far beyond the imagination. They are misleading.

Misleading results could also occur when DNP is used as indicator for cycles to failure. In the IPC report J-STD-012 (Joint Industry Standard Implementation of Flip Chip and Chip Scale Technology), assembly reliability projections were based on flip chip die being attached to the board. DNPs were used for calculation of the first failure and projection of failure with size of package. This is not valid for most CSPs, except possibly for a few wafer level CSPs without underfill. Although there is a relationship between an increase in die size and reliability, the relationship is not linear and depends on many parameters. For example, fan-out packages with small die will not follow the DNP indications.

Table 4 Misleading CSP Cycles to Failure Projections by Modeling

Package Type	I/O	Cycle Profile	Cycles to Failure Projection	Test Results
TAB CSP	46	-55/125°C	7,000	500-1,000
WAFER CSP	96	-40/125°C	3,200	200-500 8 failures
FLIP CHIP CSP	N/A	-55/125°C	20,000	N/A
LOW COST CSP	N/A	-40/125°C	21,000	N/A

LESSONS LEARNED AND RECOMMENDATIONS

Board reliability information is essential for CSP implementation for high reliability applications and to ease their use in commercial sectors. For wider application of this technology, the potential user will need design reliability data since they often do not have the resources, time, or ability to perform complex environmental characterizations. To help build the infrastructure in these areas, nearly 300 test vehicles were assembled by the JPL-led consortium to address many technical issues regarding the interplay of package types, I/O counts, PWB materials, surface finishes, and manufacturing variables for the quality and reliability of assembly packages. The following conclusions are based on the literature data analysis and comparison.

- A failure shift from solder joint to package may occur more often for miniaturized CSP packages. Projection based on the wrong failure mode result in the wrong forecast of cycles to failure.
- The board level cycles to failure of most CSP packages are comparable or better than LCC (Leadless Ceramic Chip Carrier) with similar I/O counts. These packages, however, are not as robust as conventional SM leaded packages including gull wing and J-leads. In a few cases, they might have comparable board reliability to their TSOP counterparts.
- It is much faster and enormously cheaper to simulate cycles to failure by modeling and generate unrealistic results. As examples, several unrealistic projections for CSPs were presented.
- One sources of modeling unrealistic results are the wrong assumptions for failure mechanisms. CSPs failure sources might be differ from conventional SM assemblies.
- Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with miniaturized CSPs is key to collecting meaningful test results.
- Visual inspection has been common to characterize solder quality and reject nonconformance to specification. Inspection for acceptance is still a challenge for BGAs. The challenges are further magnified for the inspection of grid CSPs with smaller features in addition to hidden solder joints. Stringent process controls are acceptable for commercial applications, but additional joint integrity verification is needed for high reliability applications. Joint integrity verification is critical to space missions.
- Availability of meaningful test results for CSPs will accelerate their use in bold technology validation space missions, and further qualification and testing will permit their use for scientific exploration missions.

REFERENCES

Four main sources of information on the text were from:
SMI '97, Proceedings of Chip Scale Packaging Symposium, SMI, Sept. 7-11, 1997
IMAPS '97, Proceedings of International Symposium on Microelectronics, Philadelphia, October 14-16, 1997
CSI '98, Proceedings of Chip Scale International, San Jose, May 6-7, 1998
ECTC '98, Proceedings of 48th Electronic Components & Technology Conference, Seattle, May 25-28, 1998

ACKNOWLEDGMENTS

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Table 1 CSPs Assembly Reliability, Flex/Rigid Interposer

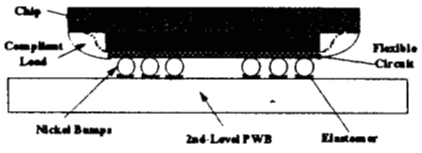
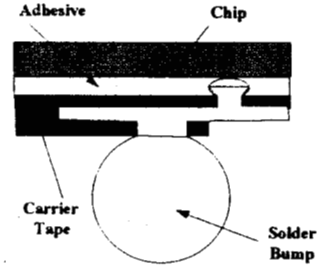
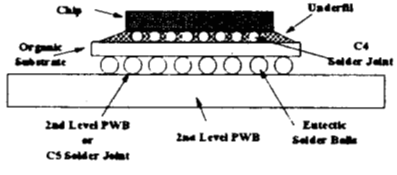
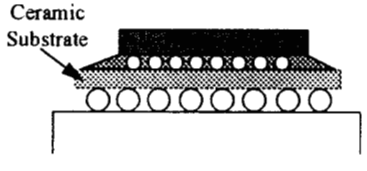
Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References
	**µBGA (Tessera) Intel Test Data**	-65°C to 150°C -55°C to 125°C	750 1000 1000 no underfill	0/78 4/78* 0/78	46	S. Greathouse," Chip Scale Package Solutions-The Pro's and Cons," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 * 4/78 right after 1,000 cycles in lead
	µBGA Motorola Test	-55°C to 125°C 5.8 cycles/hr	500* 600	1/8 3/8	40	Lall, P., "Assembly Level Reliability Characterization of Chip-Scale Packages," 48th Electronic Component & Technology Conference, May 25-28, 1998 * Internal TAB failure
	**FPBGA (NEC)**	-40°C to 125°C -55°C to 125°C 10 min. dwells -40°C to 125°C*	200 underfill 700 underfill 500 No underfill	0/20 N/A 0/12	232 208 44	S. Matsuda, K. Kata, E. Hagimoto, "Simple-Structure, Generally Applicable Chip-Scale Package," Proceeding of IEEE Electronic Components & Technology Conference, May 1995, P. 218-223 T. Oishi, et al, "Strategy for Fine Pitch BGA Development in NEC, and its Applications," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 *Presentation, CHIPCON '97
	**JACS-Pak** (Motorola)	-40°C to 125°C (1 Cycle/hr, 10 min. dwells) -55°C to 125°C Shock, 5 min. dwells	>1150* no underfil 1300**	NA 1st Failure	• 80 80	C. Koehler, et al, " A User-Focused Chip Scale Packaging Solution," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 * >600 in paper, but >1150 presentation **>1100 in paper, but 1300 1st failure presentation
	**Ceramic CSP** (Kyocera)	-40°C to 125°C	~600 no underfill, PWB 0.6mm >900 no underfill, PWB 1.6mm	NA	220	R. Lanzone, "Ceramic CSP: A Low Cost, Adaptive Interconnect, High Density Technology," Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97, Feb. 20-21, 1997 Private Communication

Table 2 SPs Assembly Reliability, Wafer Level

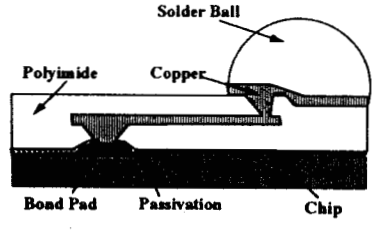
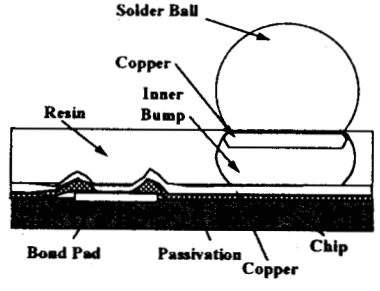
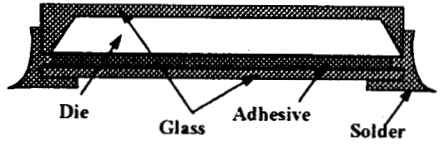
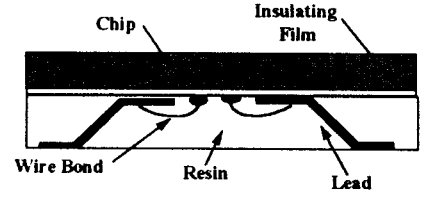
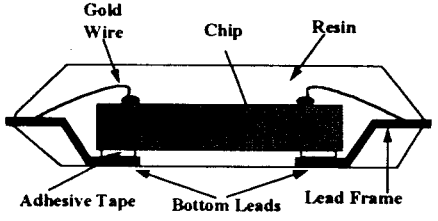
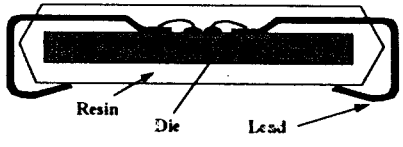
Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References.
	**miniBGA** (Sandia)	0°C to 100°C (Thermal Shock) -55°C to 125°C Thermal Shock 15 min. dwells	>2000 underfill <40 no underfilll >500 underfill	NA	266	R. Chanchani, et al, "mini Ball Gird Array (mBGA) Assembly on MCM-L Boards," Proceedings of Electronic Components and Technology Conference, May 18-21, 1997
	**Mitsubishi**	-40°C to 125°C, 1 cycle/hour	500 underfill 200 no underfill 100 bare die	0/3 (0/20) 10/30	96	S. Baba, et al, "Molded Chip Scale Package for High Pin Count," Proceeding of IEEE Electronic Components & Technology Conference, May 1996, P. 1251-1257
	**Shell Case** Peripheral	-45°C to 85°C 10 min., 1 min. between (Thermal Shock)	1000 10x10 mm die 8x13	0/24 65 µ stand off 0/40 130 µ stand off	120	Presentation- A. Badihi, "Test Results for Reliability of ShellCase CSPs," IMAPS ATW Workshop on CSP, August 10-12, 1997, Austin, Texas

Table 3 CSPs Assembly Reliability Lead On Chip

Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References
	**LOC-USON** (Fujitsu) LOC ultra-thin small outline no-lead	-65°C,30 min. to 155°C, 30 min.	500	0/40	26	J. Kasai, et al, "Low Cost Chip Scale Package for Memory Products," Surface Mount International, August 29-31, 1995
	**LOC (BLP)** LGSemicon **TSOP**	-30°C 85°C -55°C to 125°C Shock, 5 min. dwells -55°C to 125°C Shock, 5 min. dwells	>1200 800 900 900 1000	N/A 0/4 2/4 0/25 2/25	20 28 28	Y. Kim, et al, "Bottom Leaded Plastic (BLP) Package: A New Design with Enhanced Solder Joint Reliability," Proceeding of IEEE Electronic Components & Technology Conference, May 1996, P. 448-452 Y. Kim, et al, "Solder Joint Reliability of The Leaded and Leadless Packages: New BLP Design," SEMICON West, July 18-21, 1997
	**Hitachi Cable LOC**	-50°C 150°C 30 min., 10 min. between	>1000	No crack	44	K. Hatano, et al, "Reliability of CSP Manufactured by Using LOC Package Technology," IMAPS ATW Workshop on CSP, August 10-12, 1997, Austin, Texas
	**TSOP**	-55°C to 125°C -55°C to 125°C 0°C to 100°C 0°C to 100°C	2,200 200 735 750	1st Failure 1st Failure 1st Failure 1st Failure	32 32 32 32	J. Lau, editor, "Solder Joint Reliability Theory and Applications R. Darveau P. Viswanadham, et al, "Solder Joint Reliability on TSOPs-An Overview", IEEE 43rd ECTC, P 883, 1993 D. Noctor, et al, IEEE Trans on CHMT, Vol. 16, No.6, 1993